MEMS, Field Emitter, and Thermal Devices, and Structures

A Four-terminal Nanoelectromechanical Switch Based on Compressible Self-assembled Molecules

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Sponsorship: NSF

Nanoelectromechanical (NEM) switches are under investigation as complements to, or substitutes for, CMOS switches owing to their intrinsic quasi-zero static leakage, large ON-OFF conductance ratio, and high robustness in harsh environments. For most NEM contact switches, a trade-off between high actuation voltage and the risk of stiction failure seems inevitable due to the strong van der Waals attraction between contacts at the nanoscale. This attraction leads to unfavorable dynamic power consumption and decreased reliability. Through this research, we have developed a novel tunneling NEM switch, termed a "squitch", based on a metal-molecule-metal junction whose tunneling gap can be modulated by compressing the molecule layer with electrostatic force created by a voltage applied between the metal electrodes. In contrast to conventional NEM contact switches, direct contact of squitch electrodes in the ON state is avoided by assembling a molecular spacer between the electrodes; the molecular spacer acts to hold the squitch together and helps reduce hysteresis and the possibility of stiction failure.

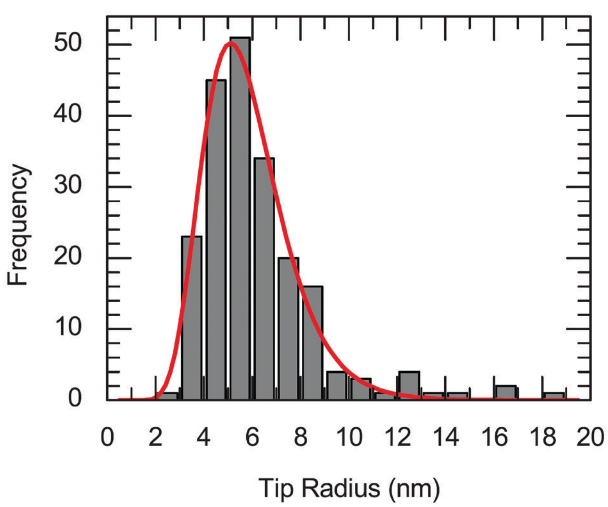
A multi-terminal squitch has been demonstrated using a chemically-synthesized Au nanorod as a floating top electrode, and bottom Au electrodes patterned with electron beam lithography. With the help of a peeling technique that we have developed, Au electrodes are created with sub-nanometer roughness. The electrodes include two actuation gates recessed by several nanometers via a graphene sacrificial layer. By choosing molecules with appropriate chain lengths, we are able to define nanometer-wide electrode-to-nanorod gaps, which can be subsequently adjusted by a bias voltage applied between the gate electrodes. With a proper bias voltage, we can exponentially modulate the conduction current through a small variation of the gating voltage. Our squitch has been experimentally demonstrated to exhibit low actuation voltage and hysteresis, which supports its prospects in ultra-low power logic applications.

Highly Uniform Silicon Field Emitter Arrays

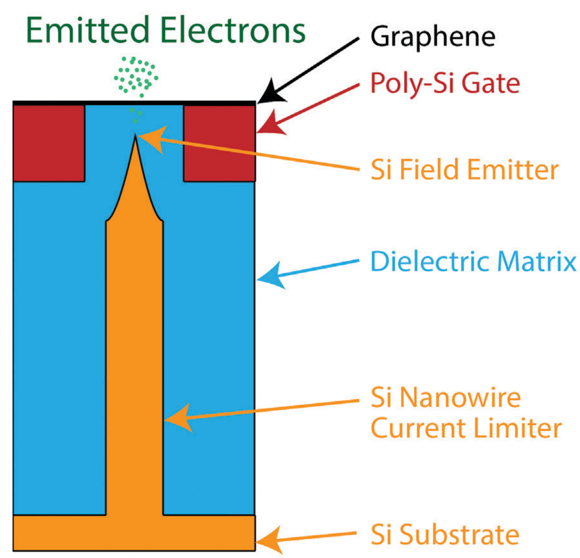
N. Karaulac, A. I. Akinwande
Sponsorship: DARPA, IARPA

Cold cathodes based on silicon field emitter arrays (FEAs) have shown promising potential in a variety of applications requiring high current density electron sources. However, FEAs face a number of challenges that have prevented them from achieving widespread use in commercial and military applications. One problem limiting the reliability of FEAs is emitter tip burnout due to Joule heating. The current fabrication process for FEAs results in a non-uniform distribution of emitter tip radii. At a fixed voltage, emitters with a small radius emit a higher current while emitters with a large radius emit a lower current. Therefore, emitters with a small radius reach their thermal limit due to Joule heating at lower voltages and consequently burnout. Previous solutions to mitigating tip burnout have focused on limiting the emitter current with resistors, transistors, or nanowires in order to obtain more uniform emission current.

In this project, we focus on increasing the uniformity of emitter tip radii as a means to reduce tip burnout. Figure 1 shows a typical distribution of emitter tip radii for FEAs. The non-uniform distribution of emitter tip radii first forms during the photolithography step that defines the array of "dots" which become the etching mask for the silicon tips. In our FEA fabrication process, we use a tri-level resist process that nearly eliminates the light wave reflected at the photoresist/silicon interface, and hence improves the uniformity of the dot diameter. Furthermore, we integrate the emitter tips with silicon nanowires to improve their reliability. Figure 2 shows a diagram of the fabricated structure. We expect our fabrication process to result in FEAs with more uniform emission current and potentially longer lifetime.



▲ Figure 1: Non-uniform distribution of emitter tip radii resulting from the fabrication process of silicon FEAs.



▲ Figure 2: Cross-sectional diagram of a silicon field emitter. The emitter tip sits on top of a high-aspect-ratio silicon nanowire that limits the field emission current from the tip.

FURTHER READING

- S. A. Guerrera and A. I. Akinwande, "Nanofabrication of Arrays of Silicon Field Emitters with Vertical Silicon Nanowire Current Limiters and Self-aligned Gates," *Nanotechnology*, vol. 27, no. 29, pp. 295302:1-11, Jul. 2016.
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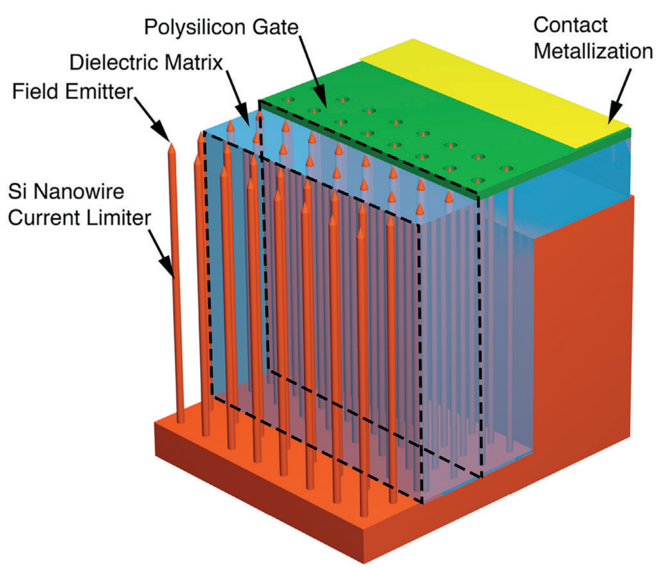
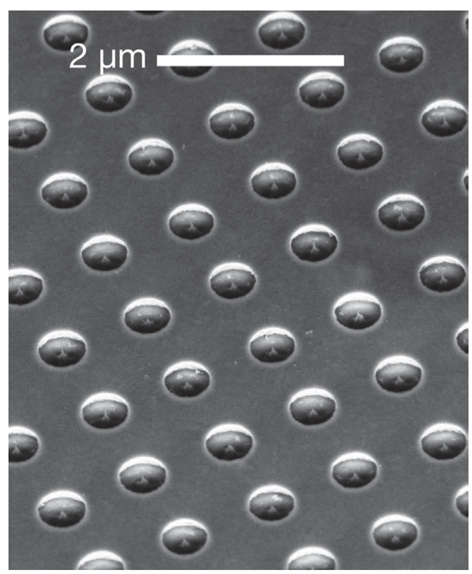
A Silicon Field Emitter Array as an Electron Source for Phase Controlled Magnetrons

W. Chern, J. Browning, A.I. Akinwande
Sponsorship: AFOSR

Magnetrons are a highly efficient (>90%), high-power vacuum-based microwave source. In a magnetron, free-electrons in vacuum are subject to a magnetic field while moving past open metal cavities, resulting in resonant microwave radiation to be emitted. Current state-of-art magnetrons use a heated metal filament to thermionically emit electrons into vacuum continuously and are not addressable. This work seeks to replace the heated metal filament as a source of electrons with silicon field emitter arrays in order to improve the efficiency and increase the power, especially when several sources are combined. Silicon field emitter arrays, schematically shown in Figure 1, are devices that are normally off and are capable of high current densities plus spatial and temporal addressing. These arrays consist of many sharp tips made of silicon sitting on long silicon nanowires that limit the current of the electron emission. Electrons from the silicon tip tunnel into a vacuum as a result of the high electric field of the applied bias on the polysilicon gate. Pulsing the electric field applied on the gate can turn the arrays on and off. The proposed use of silicon field emitter arrays in a magnetron will allow injection locking and hence phase control of magnetrons. Phase-controlled magnetrons have multiple applications in areas where high- power microwave sources are desired. Currently, Si field emitter arrays have been designed for the magnetron and are undergoing testing with collaborators at Boise State University.





▲ Figure 1: (Left) 3-D rendering of Si device structure. For clarity, layers have been omitted in different regions of the rendering to show detail. In the front, the bare silicon nanowires [200-nm diameter & 10-µm height] with sharp tips. (Right) Top-view of a fabricated device with 350-nm gate aperture and 1-µm tip-to-tip spacing.

FURTHER READING

- S. Guerrera and A. I. Akinwande, “Silicon Field Emitter Arrays with Current Densities Exceeding 100 A/cm2 at Gate Voltages Below 75 V,” *Proceedings of IEDM*, 2016.

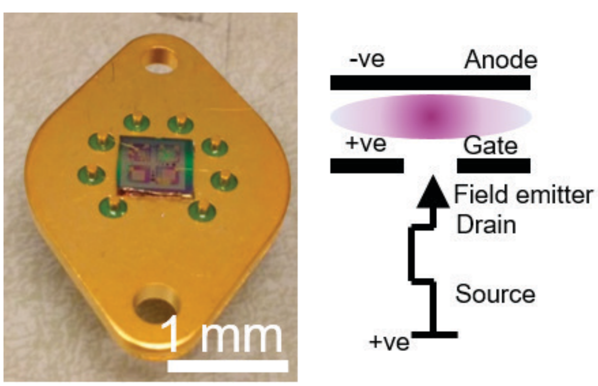
Silicon Field Ionization Arrays Operating > 200 V for Deuterium Ionizers

G. Rughoobur, A. I. Akinwande
Sponsorship: DARPA

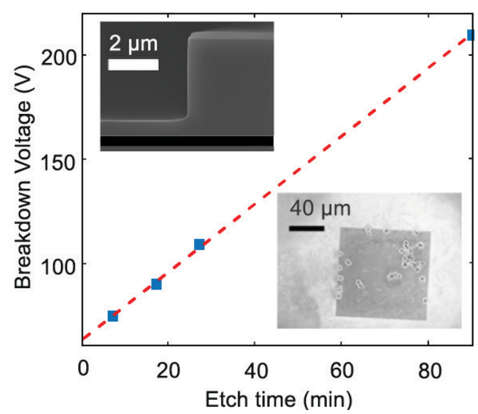
Devices that can field-ionize gas molecules at low bias voltages are essential for many applications such as ion mobility spectrometry and highly selective portable gas sensing. Field ionization consists of a valence electron of a gas atom or molecule tunneling through a potential barrier, commonly into a vacant energy state of the conduction band of a metal at the anode. Classic ion sources require extremely high positive electric fields, of the order of 10^8 volts per centimeter. Such fields are only achievable in the vicinity of very sharp electrodes under a large bias. Ion sources based on microwave plasma generation have demonstrated high currents and high current densities. Yet, they are bulky and require large magnetic fields. Alternatively, single or arrays of gated tip structures have been used as field ionizers, but they emit low currents (~10 nA). Early tip burn-out due to non-uniform tip distribution and low voltage breakdown are the two main causes of such low currents.

In this work, Si field ionization arrays (FIAs) with a unique device architecture that uses a high-aspect-ratio (~50:1) silicon nanowire current limiter to regulate electron flow to each field emitter tip in the array is proposed. The nanowires are 10 µm in height, 1 µm apart and 100-200 nm in diameter. A dielectric matrix of (Si_3N_4/SiO_2) supports a poly-Si gate while a 3 µm thick dielectric holds the contacts. Current densities >100 A/cm^2 and lifetime > 100 hours have already been reported. The tip radius has a log-normal distribution varying from 2 to 8 nm with a mean of 5 nm and a standard deviation of 1.5 nm, while the gate aperture is ~350 nm. Field factors, β, > 1 × 10^6 cm^{-1} can be achieved with these devices implying that voltages of 250-300 V (if not less) can produce D^+ ions based on the tip field of 25-30 V/nm. Completed chips on a package are shown in Figure 1 together with a schematic of the test set-up for field ionization.

Breakdown at the mesa edge at voltages ~70 V was the reported by Guerrera, et al. However this has now been overcome by etching a vertical sidewall profile (Figure 2) with a combination of both SF_6 and C_4F_8 flowing simultaneously (Figure 2). I-V characterization in air demonstrates breakdown occurs within the active region (Figure 2) possibly due to the narrow gate apertures and the short oxide thickness from the tip to the poly-Si gate. Initial results show that further etching this oxide to expose the nanowire increases the oxide separation to the gate, which in turns increases the breakdown voltage (Figure 2), thus enabling the Si FIAs to be operated at voltages exceeding 200 V.



▲Figure 1: (Left) Wirebonded Si FIA device onto a TO3 package ready for field ionization, (Right) Schematic of current limiter integrated Si FIA and required electric potential for ionization.



▲Figure 2: (Top Left) Vertical mesa profile to prevent early breakdown, (Main) Breakdown voltage in air as a function of oxide etch time to expose Si tips, (Bottom Right) Locations of breakdown spots.

FURTHER READING

- S. A. Guerrera and A. I. Akinwande, "Silicon Field Emitter Arrays with Current Densities Exceeding 100 A/cm2 at Gate Voltages Below 75 V," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 96–99, Jan. 2016.
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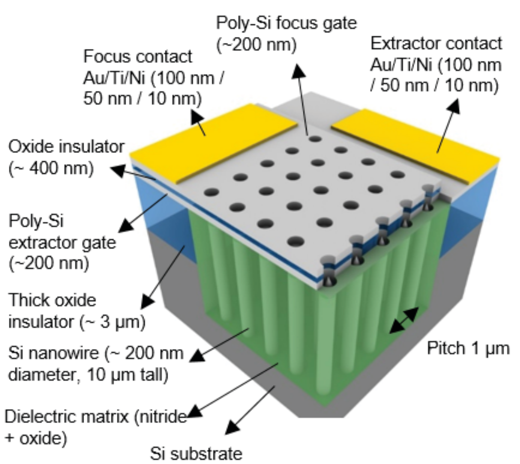
High Current Density Silicon Field Emitter Arrays (FEAs) with Integrated Extractor and Focus Gates

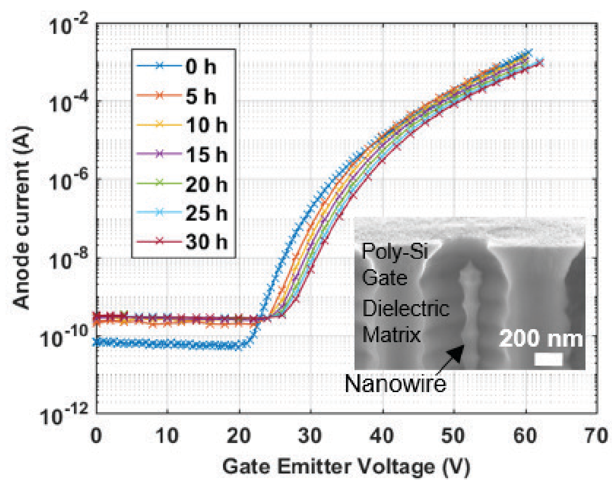
G. Rughoobur, A. I. Akinwande
Sponsorship: AFRL/IARPA

Cold electron sources have been identified as alternatives to thermionic emitters due to their lower operating temperature, instant response to the applied electric field, and their exponential current-voltage characteristics. With the advent of microfabrication, the generation of high electric fields around sharp emitters to tunnel electrons was made possible. Scalable and high-density field emitter arrays (FEAs) based on Si are advantageous due to compatibility with CMOS processes, maturity of technology, and the ease to fabricate sharp tips using oxidation. The use of a current limiter is necessary to avoid burning of the sharper tips; active method using an integrated MOSFET, or passive methods using a nanopillar (~200 nm wide, 10 µm tall) in conjunction with the tip has been demonstrated. Si FEAs reported by Guerrera, et al., exhibited high current densities exceeding 100 A/cm² and having lifetimes of over 100 hours.

The need for another gate (Figure 1) becomes essential to control the focal spot size of the beam as the tips become blunt with time and as a consequence, the turn-on voltage also increases (Figure 2). With the focus electrode, stray electrons extracted by the gate closest to the tip will be captured and only electrons emitted within a certain cone angle will reach the anode, thus achieving a narrower focal spot size compared to a single gated Si FEA. The voltage on the focus gate can be varied with time to maintain a fixed focal spot size or even as an electron control switch. Indeed having a high positive focus voltage pulls all the extracted electrons and can be used to prevent electrons reaching the anode. This also offers the opportunity for fast switching of these Si FEAs, which has been a limitation thus far of these devices. In this work we are optimizing the process steps to fabricate Si FEAs with the two integrated gates and current limiter, to characterize the effects of the focus gate on electron emission. These devices will find applications in flat panel displays, nanofocused X-ray sources, microwave tubes, and triodes.



▲ Figure 1: Si field emitter array with integrated current limiter, self-aligned extractor and focus gates for nanofocused cold electron sources.



▲ Figure 2: Electrical characterization with only extractor gate measured over a period of 30 hours for a 500 by 500 array of Si FEAs, inset shows SEM image of Si FEA with a single gate and current limiter exposed by removing oxide.

FURTHER READING

- S. A. Guerrera and A. I. Akinwande, "Silicon Field Emitter Arrays with Current Densities Exceeding 100 A/cm2 at Gate Voltages Below 75 V," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 96–99, Jan. 2016.
- S. A. Guerrera and A. I. Akinwande, "Nanofabrication of Arrays of Silicon Field Emitters with Vertical Silicon Nanowire Current Limiters and Self-aligned Gates," *Nanotechnology*, vol. 27, no. 29, pp. 295302, Jul. 2016.
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Carbon Nanotubes Based-field Emitters by 3-D Printing

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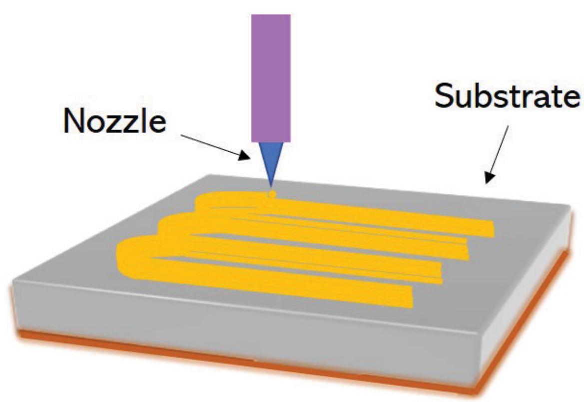
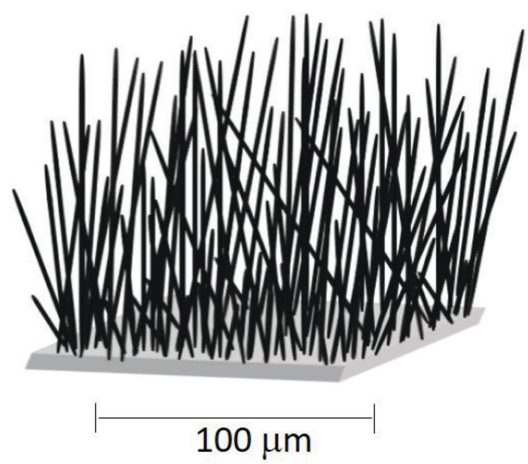
Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program

In field emission, electrons are ejected from a solid surface via quantum tunneling due to the presence of a high local electrostatic field. Compared to state-of-the-art thermionic electron sources, field emission cathodes consume significantly less power, are faster to switch, and could operate at higher pressure. Field emission cathodes have a wide range of applications such as X-ray sources, flat-panel displays, and electron microscopy.

Several materials, e.g., Si, ZnO, and graphene, have been explored as field emission sources; however, carbon nanotubes (CNTs) are very promising to implement field emission cathodes due to their high aspect ratio, high electrical conductivity, excellent mechanical, and chemical stability, and high current emission density. Reported approaches for fabricating CNT field emitters include screen printing and direct growth of nanostructures (e.g., plasma-enhanced chemical vapor deposition) where a static stencil, i.e., mask, is involved to produce patterned structures in specific locations. These masks increase the time and cost needed to iterate the pattern, affecting the prototype optimization of the cathode. Ink direct writing (IDW), i.e., the creation of imprints by extrusion of liquid suspensions through a small nozzle, has emerged as an attractive maskless patterning technique that can accommodate a great variety of materials to create freeform imprints at low-cost (Figure 1). An imprint with CNTs protruding from the surface of the imprint (Figure 2), strongly adhered to the substrate can achieve stably high-current emission when an electric field is applied. We are currently working on the design and optimization of the formulation of a CNT-based ink, to eventually demonstrate low-cost field emission sources.



▲ Figure 1: Example of a pattern 3-D printing by means of ink direct writing using a paste made of a filler dispersed into an organic matrix.



▲ Figure 2: Example of an array of porous structure of carbon nanotubes bristling adhered to the substrate showing the tip of CNTs are exposed.

FURTHER READING

- A. P. Taylor and L. F. Velásquez-García, “Electrospray-printed Nanostructured Graphene Oxide Gas Sensors,” *Nanotechnology*, vol. 26, no. 50, pp. 505301:1-8, Dec. 2015.
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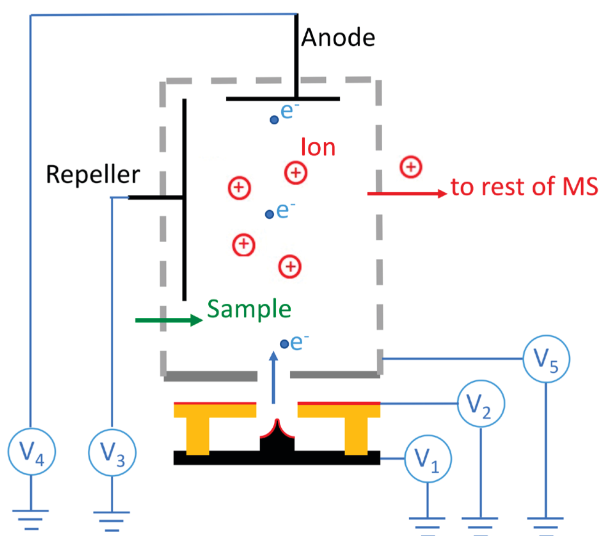
- L. F. Velásquez-García, B. Gassend, and A. I. Akinwande, “CNT-based MEMS Ionizers for Portable Mass Spectrometry Applications,” *J. of Microelectromechanical Systems*, vol. 19, no. 3, pp. 484 - 493, Jun. 2010.

Electron Impact Gas Ionizer with 3-D Printed Housing and NEMS Si Field Emission Cathode for Compact Mass Spectrometry

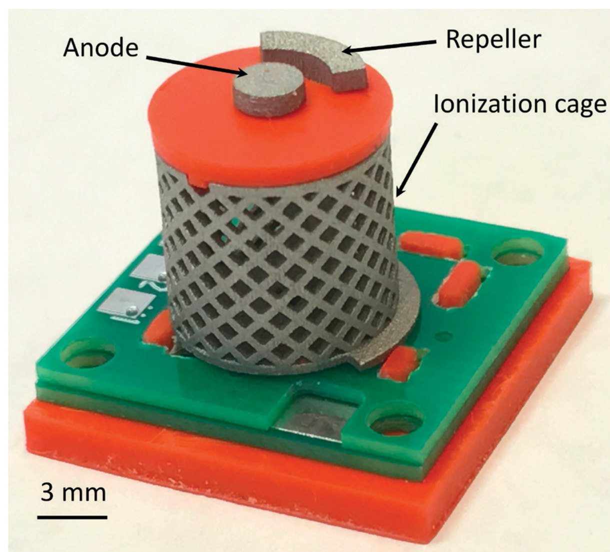
C. Yang, L. F. Velásquez-García
Sponsorship: IARPA

Mass spectrometry is widely used to quantitatively determine the composition of samples. However, the bulky size and high-power consumption of conventional mass spectrometry instruments limit their portability and deployability. One of the key components of a mass spectrometer (MS) is the ionizer. State-of-the-art electron impact gas ionizers use a stream of electrons produced by a thermionic cathode to create ions by fragmentation. Field emission cathodes, based on quantum tunneling of electrons triggered by high electrostatic fields, are a better alternative for portable mass spectrometry of gases compared to mainstream thermionic cathodes because they consume significantly less power, are faster to switch, and could operate at higher pressure.

In this project, we are developing a compact electron impact gas ionizer based on a cleanroom-microfabricated cathode and a 3-D printed ionization housing (Figure 1). The cathode is an array of nano-sharp silicon field emitters with proximal, self-aligned extractor gate, while the ionization housing is composed of an ionization region surrounded by an ionization cage, an anode electrode, a repeller electrode, and a dielectric structure that holds together the electrodes. To produce ions (i) a high enough bias voltage is applied between the extractor gate and the silicon tips, shooting electrons into the ionization region, (ii) the anode electrode attracts the emitted electrons, forcing them to interact with the neutral gas molecules within the ionization region, (iii) the bias voltage of the ionization cage maximizes the ionization yield of the interaction between the electrons and the neutral gas molecules, and (iv) the repeller electrode pushes ions out of the ionization cage. Figure 2 shows an assembled ionizer. Current work is focused on characterization of the field emission cathode and gas ionizer at various conditions.



▲ Figure 1: Schematic of electron impact gas ionizer with field emission cathode. The ions produced by the device are fed to the rest of the MS.



▲ Figure 2: Picture of implemented gas ionizer. The field emitter array chip is mounted between two printed circuit boards.

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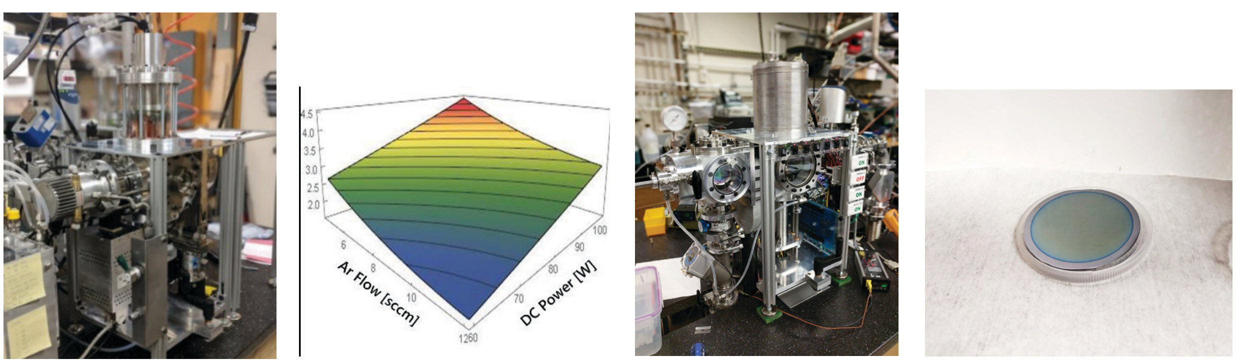
- L. F. Velásquez-García, B. Gassend, and A. I. Akinwande, "CNT-based MEMS Ionizers for Portable Mass Spectrometry Applications," *J. Microelectromech. Syst.*, vol. 19, no. 3, pp. 484-493, June 2010.

Development of a Tabletop Fabrication Platform for MEMS Research, Development, and Production

M. D. Hsing, P. A. Gould, M. A. Schmidt
Sponsorship: MTL

A general rule of thumb for new semiconductor fabrication facilities (fabs) is that revenues from the first year of production must match the capital cost of building the fab itself. With modern fabs routinely exceeding $1 billion to build, this rule serves as a significant barrier to entry for research and development and for groups seeking to commercialize new semiconductor devices aimed at smaller market segments and requiring a dedicated process. To eliminate this cost barrier, we are working to create a suite of tools that will process small (~1") substrates and cumulatively cost less than $1 million. This suite of tools, known colloquially as the 1" Fab, offers many advantages over traditional fabs. By shrinking the size of the substrate, we trade high die throughputs for significant capital cost savings, as well as substantial savings in material usage and energy consumption. This substantial reduction in the capital cost will drastically increase the availability of semiconductor fabrication technology and enable experimentation, prototyping, and small-scale production to occur locally and economically.

Our research in the last few years has been primarily focused on developing and characterizing tools for the 1" Fab. In previous years, we demonstrated a deep reactive ion etching (DRIE) tool and a corresponding modular vacuum tool architecture, and we are now working to develop a reactive magnetron sputtering tool and an inductively coupled plasma-based PECVD tool (ICP-CVD) for depositing a wide variety of materials. The reactive magnetron sputtering tools operates using a 2" target and a direct sputtering configuration and is fully integrable with the modular tool architecture of the 1" Fab. We have demonstrated the functionality of the tool with the depositions of copper, aluminum, and via reactive sputtering, aluminum nitride. The system has been characterized using a response surface methodology and consistent, uniform depositions with <6% variation across the wafer have been shown. The ICP-CVD tool has also been built within the modular tool architecture and is being tested with depositions of SiO_2, SiN_x, and a-Si. The use of an ICP source allows depositions to occur at temperatures as low as 25°C, with low hydrogen incorporation, and quality approaching that of LPCVD depositions. Film stress and index of refraction are also controllable.



(a) (b) (c) (d)

▲ Figure 1: (a) 1" Fab Sputtering Tool; (b) Aluminum RSM for sputtering tool; (c) 1" Fab ICP-CVD tool; (d) ICP-CVD SiO_2 film on 2" wafer.

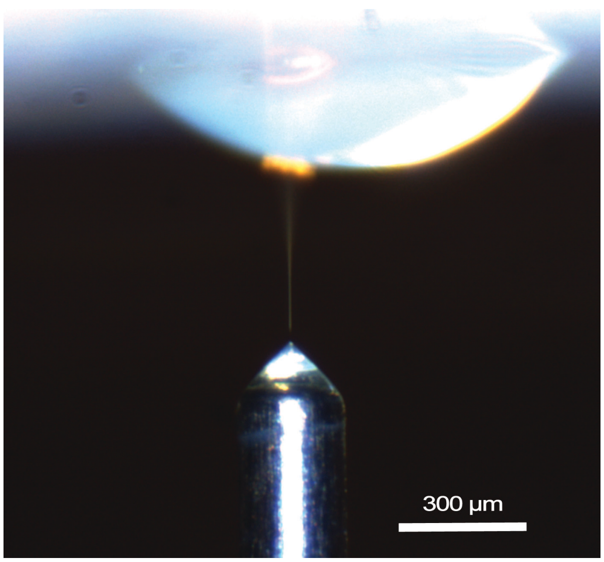
Printed Piezoelectric Thin Films via Electrohydrodynamic Deposition

B. García-Farrera, L. F. Velásquez-García
Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program

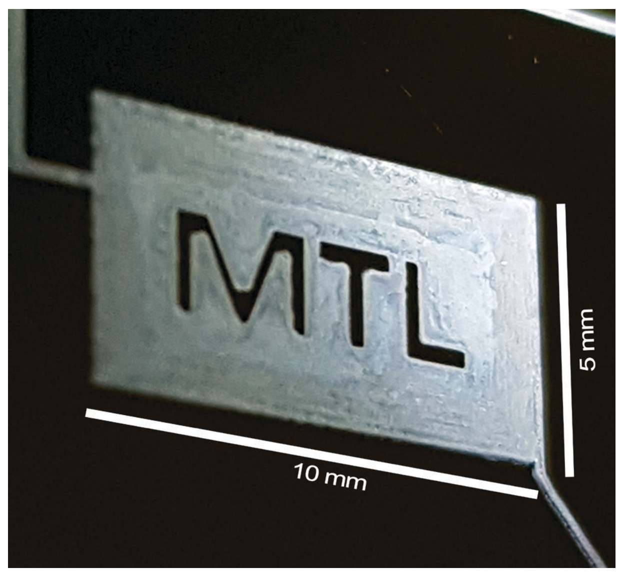
Piezoelectric components have found applications in a variety of fields including energy harvesting, biological and chemical sensing, and telecommunications. The creation of piezoelectric thin films has made possible the implementation of exciting devices that operate at higher frequency (a consequence of the reduction of the thickness of the piezoelectric material) including highly sensitive gravimetric biosensors and acousto-fluidic actuators. However, traditional manufacturing methods for piezoelectrics require a high vacuum, show low deposition rates, involve expensive and complex equipment, and require additional microfabrication processes to achieve the required geometries via patterning and lithography.

Electrohydrodynamic deposition harnesses the electrospray phenomenon to create ultrathin imprints from liquid feedstock (Figure 1). When the electrospray emitter operates in the cone-jet mode, stable jetting of the liquid feedstock allows for the direct writing of structures, thus, eliminating the need for steps for material removal, e.g., mask transfer and etching (Figure 2). In addition, electrohydrodynamic deposition can operate at room temperature without the need for a vacuum and can be scaled-up via electrospray emitter multiplexing.

This project aims to produce piezoelectric thin films suitable for acoustic resonators and actuators via electrospray jetting of nanoparticle-doped liquid feedstock. Initial work revolved around the optimization of the deposition parameters and formulation of the liquid feedstock for the reduction of the printed line's width and thickness, elimination of the "coffee ring" effect, and analysis of the crystallographic orientation of the films. Current work focuses on improving the film's homogeneity, increasing the crystal orientation towards a highly oriented film, and its piezoelectric characterization and application as a sensor.



▲ Figure 1: Electrospray of nanoparticle-doped liquid feedstock. The electric field from the bias voltage between the capillary and the substrate ejects a fine jet of solution from the apex of the Taylor cone.



▲ Figure 2: Negative of the Microsystems Technology Laboratory logo printed with piezoelectric liquid feedstock via electrospray.

FURTHER READING

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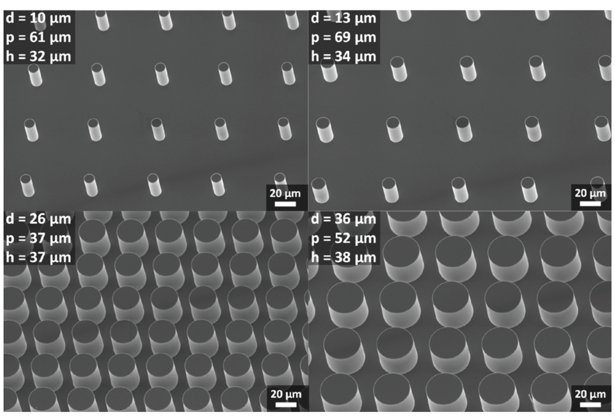
- L. F. Velásquez-García, "SLA 3-D-Printed Arrays of Miniaturized, Internally-fed, Polymer Electrospray Emitters," *J. of Microelectromechanical Systems,* vol. 24, no. 6, pp. 2117–2127, Dec. 2015.

Is the Surface Wickability the Single Descriptor of Critical Heat Flux during Pool Boiling?

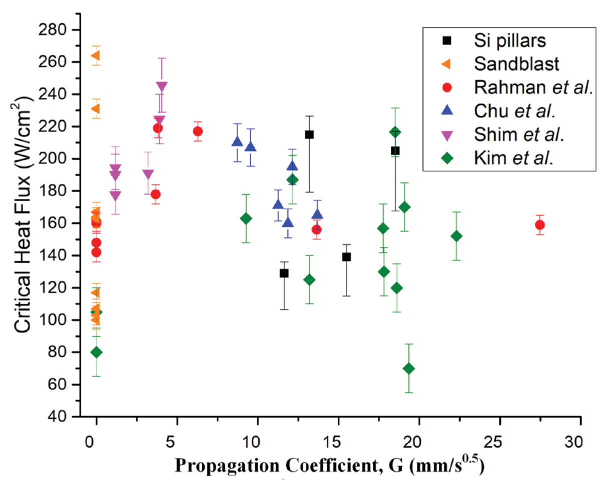
Y. Song, Y. Zhu, D. J. Preston, H. J. Cho, Z. Lu, E. N. Wang
Sponsorship: Exelon Corporation

Enhancement and estimation of critical heat flux (CHF) are two of the most important research areas of pool boiling. It is well-known that microstructured surfaces can extend the limit of CHF up to ~250% higher than that of a flat surface. The mechanism for this enhancement has generally been accepted as the wickability of structured surfaces originating from liquid propagation within the surface structures driven by capillary pressure. We investigated the applicability of this theory based on the accumulated data of previous studies and our experimental data. We first calculated capillary pressure and permeability of structured surfaces to characterize liquid propagation rate analytically. We then performed pool boiling experiments on silicon micropillar surfaces to measure CHF values.

We found that there is no distinct relationship between the CHF and wickability contrary to a general notion. Our results suggest that although liquid wicking has been found to be important, the parameter wickability defined by previous works alone is not sufficient to describe CHF. In addition to the wickability, we propose that there may be other important parameters that also change along with the surface structures, e.g., the diameter of vapor columns and bubble departure size, among others, which need further investigation.



▲ Figure 1: SEM images of the fabricated silicon microstructured surfaces. A 300 nm-thick thermal oxide layer was grown to enhance surface wettability. d, p, and h represent the diameter, pitch (center-to-center distance), and the height of pillar arrays, respectively.



▲ Figure 2: Critical heat flux as a function of wickability characterized by the propagation coefficient. The propagation coefficient dictates the speed of liquid propagation within the structured surfaces.

FURTHER READING

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Gravitationally-driven Wicking Condensation

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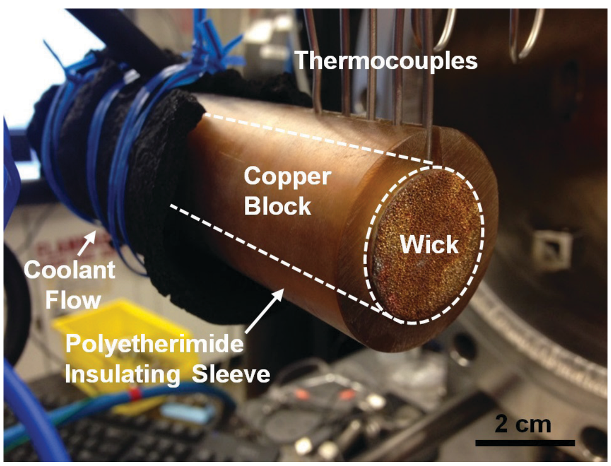
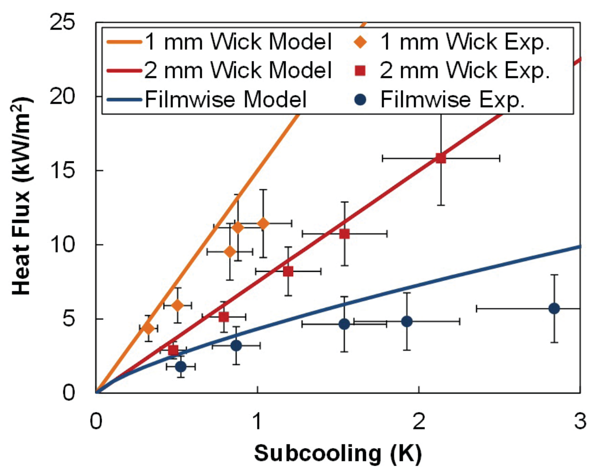
Sponsorship: Abu Dhabi National Oil Company, ONR, NSF, AFOSR

Vapor condensation is routinely used as an effective means of transferring heat or separating fluids. Filmwise condensation, where the condensate completely covers the condenser surface, is prevalent in typical industrial-scale systems. Dropwise condensation, where the condensate forms discrete liquid droplets, can improve heat transfer performance by an order of magnitude compared to filmwise condensation; however, current state-of-the-art dropwise technology relies on functional hydrophobic coatings, which are often not robust and therefore undesirable in industrial conditions. Furthermore, low surface tension condensates, like hydrocarbons, pose a unique challenge since coatings used to shed water often do not repel these fluids.

We demonstrated a method to enhance condensation heat transfer using gravitationally-driven flow through a porous metal wick, which takes advantage of the condensate's affinity to wet the surface and also eliminates the need for condensate-phobic coatings. The condensate-filled wick has a lower thermal resistance than the fluid film observed during filmwise condensation, resulting in an improved heat transfer coefficient of up to an order of magnitude and comparable to that observed during dropwise condensation. The improved heat transfer realized by this design presents the opportunity for significant energy savings in natural gas processing, thermal management, heating and cooling, and power generation.



▲ Figure 1: The experimental test fixture shown here was used to calculate the heat flux and surface temperature. The copper block was insulated by a polyetherimide sleeve (interface indicated with white dashed lines) to prevent condensation on the sidewalls and generate a linear, one-dimensional temperature profile within the block. The experiment was conducted in a controlled environmental chamber in which noncondensable gases were removed, and the condensing fluid was introduced as vapor with a known temperature. The copper wick was attached to the front of the copper block by diffusion bonding.



▲ Figure 2: Experimental results (points) are plotted with model predictions (solid lines) for the 1-mm and 2-mm-thick copper foam wicks tested in the present work, as well as for filmwise condensation on a flat copper surface, with pentane as the condensate; the experimental results are in good agreement with the model predictions. Wicking condensation outperformed filmwise condensation by over 350% in the experimental analysis, and is expected to achieve up to an order of magnitude enhancement at higher subcooling based on the modeling results.

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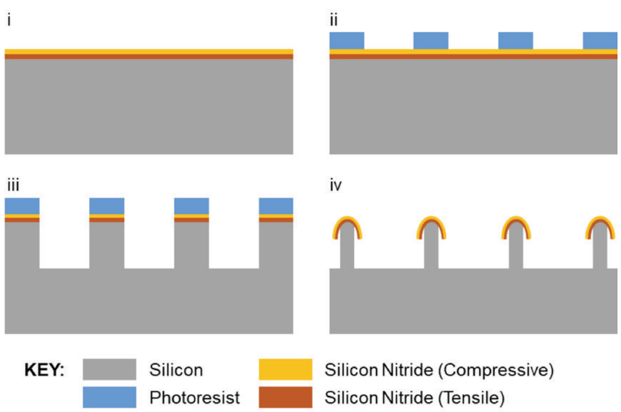
A Simple Fabrication Method for Doubly Reentrant Omniphobic Surfaces via Stress Induced Bending

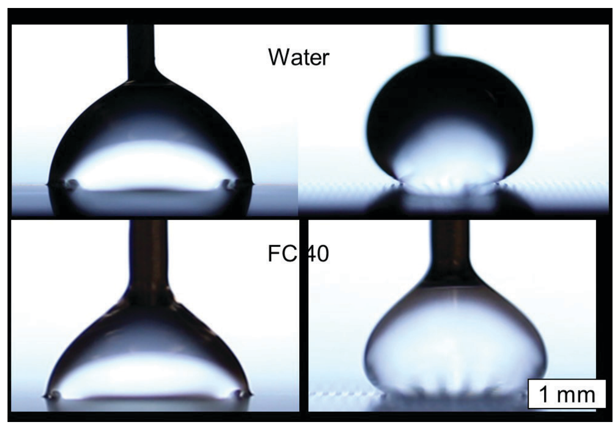
K. L. Wilke, M. Garcia, D. J. Preston, E. N. Wang
Sponsorship: Masdar Institute of Science and Technology

We developed omniphobic, doubly reentrant surfaces fabricated with a simple method suitable for use with traditional microfabrication processes. Intrinsic stresses in deposited layers of silicon nitride induced bending of a singly reentrant microstructure, creating the doubly reentrant geometry. Due to the use of standard microfabrication processes, this approach may be extended to a variety of materials and feature sizes, increasing the viability of applying omniphobic doubly reentrant structures for use in areas such as superomniphobicity, anti-corrosion, heat transfer enhancement, and drag reduction.

Figure 1 shows the fabrication process, in which standard photolithography and etches used to create singly reentrant microstructures are adopted. However, due to the stresses in deposited layers of silicon nitride, the singly reentrant structure is bent into a doubly reentrant geometry that renders the surface omniphobic. Figure 2 shows the contact angle of water and FC 40 on the surface. FC 40 has a much lower surface tension than water, which typically makes it difficult to repel. However, due to the double reentrant geometry of this surface, it is repelled.



▲Figure 1: Fabrication method of doubly reentrant structures. i: Deposition of films with tensile and compressive stress. Silicon nitride was deposited with PECVD in this study. The film stresses induce bending in the final fabrication step to create the doubly reentrant geometry. Stresses and film thicknesses were chosen based on modeling of the bending. ii: Etch mask defined using standard photolithography. iii: Deep reactive ion etch (DRIE) of structures. iv: Isotropic silicon etch with SF6 in the DRIE to create doubly reentrant feature due to stress induced bending.



▲Figure 2: Images of advancing contact angle on the stripe-textured hoodoo surface, both parallel and perpendicular to the stripe for both water and FC 40. Both fluids were repelled due to the surface omniphobicity.

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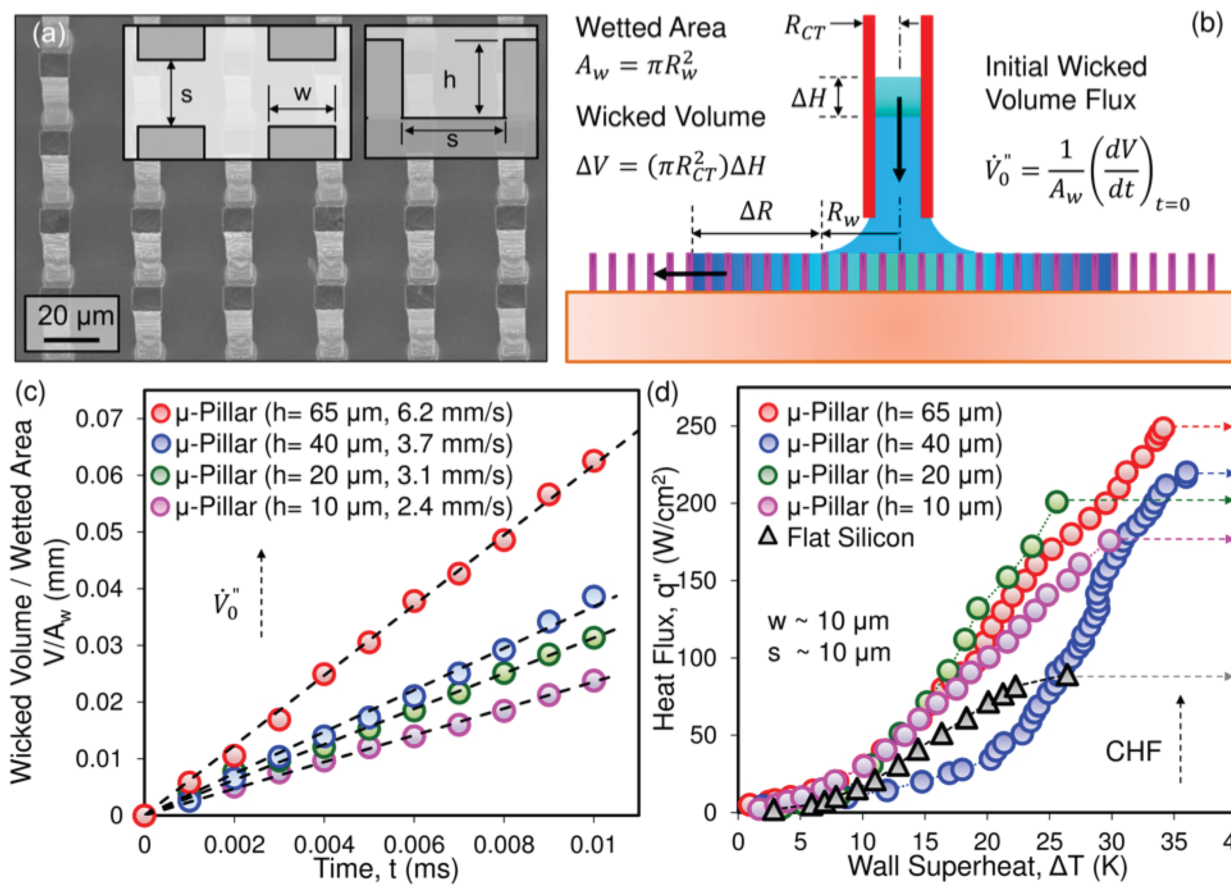
Micro-engineered Pillar Structures for Pool Boiling Critical Heat Flux Enhancement

M. M. Rahman, C. Wang, J. Ge, M. Bucci, J. Buongiorno
Sponsorship: Exelon Corporation, MISTI

Increasing the performance of phase-change heat transfer phenomena is key to the development of next-generation electronics, as well as power generation systems and chemical processing components. Surface-engineering techniques could be successfully deployed to achieve this goal. For instance, by engineering micro/nano-scale features, such as pillars, on the boiling surface, it is possible to attain 100% enhancement in pool boiling critical heat flux (CHF). Researchers have been working on several CHF enhancing micro- and nano-structured surfaces for years. However, due to the complexity of CHF phenomena, there is still no general agreement on the enhancement mechanism. An investigation of the effect of micropillar height on surface capillary wicking and the associated pool boiling CHF enhancement has been conducted. Several 1 cm × 1 cm silicon micropillar surfaces with different micro-pillar heights have been fabricated using MTL's photolithography and DRIE facilities.

The surfaces were characterized using MTL's Scanning Electron Microscope (SEM), as shown in Figure 1a. The surfaces were then characterized by measuring the capillary wicking rate using high-speed imaging and a custom-built capillary tube approach as presented in Figure 1b. The capillary wicking experimental results are presented in Figure 1c is demonstrating the increase in liquid transport capability by increasing the micro-pillar heights.

Finally, the performances of such structures were characterized through traditional pool boiling experiments and compared with a flat silicon heater (Figure 1d). The surfaces were tested at atmospheric pressure and saturation temperature using DI water as the working fluid. The results demonstrate the benefits of wicking promoted by these structures in terms of CHF enhancement.



▲ Figure 1: Microstructured surfaces for CHF enhancement. (a) SEM image of a fabricated surface, (b) schematic of wicking experiment, (c) experimental wicking results, and (d) pool boiling result of microstructured surfaces compared to flat silicon reference surface.

Boron Arsenide Crystals with High Thermal Conductivity and Carrier Mobility

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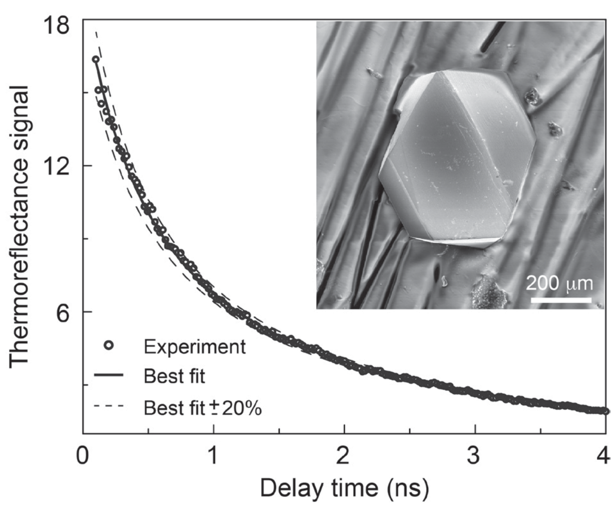
Sponsorship: ONR MURI, DOE S3TEC

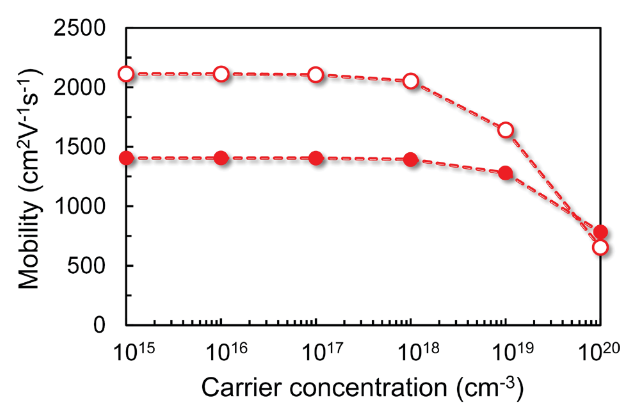
Overheating presents a major challenge in modern electronics industry due to the increasingly higher power density. High temperatures not only limit device performance, but also greatly reduce reliability and lifetime. To effectively dissipate heat from an electronic chip, materials with high thermal conductivity (k) are crucial. Common electronic materials such as copper and silicon exhibit a room temperature (RT) k of 401 $Wm^{-1}K^{-1}$ and 148 $Wm^{-1}K^{-1}$, respectively. In comparison, diamond holds the current k record of about 2000 $Wm^{-1}K^{-1}$ at RT. However, natural diamond is scarce, and synthetic diamond still suffers from slow growth, low quality, and high cost. In addition, significant thermal stresses can arise from the large mismatch in the coefficient of thermal expansion between diamond and common semiconductors.

Recently, first-principles calculations predicted a very high RT k of about 1400 $Wm^{-1}K^{-1}$ for cubic boron arsenide (BAs), rendering it a close competitor for diamond. Our materials collaborators from the University of Houston and UCLA have grown samples of different sizes and qualities. We carried out thermal transport measurement of these sub-millimeter to millimeter-sized samples using time-domain thermoreflectance (TDTR) (Figure 1), among other methods. In some samples, we have reached thermal conductivity as high as 1200 $Wm^{-1}K^{-1}$.

We have also carried out the first-principles calculation of electron and hole mobility in boron-based III-V materials. We predict that BAs has both high electron (1400 $cm^2V^{-1}s^{-1}$ at RT) and hole (2110 $cm^2V^{-1}s$-1 at RT) mobility (Figure 2). These characteristics, together with the high thermal conductivity, make BAs attractive for microelectronics applications both as device materials and as heat sink materials.



▲ Figure 1: A cubic BAs crystal grown via seeded chemical vapor transport is shown in the inset. A thermal conductivity up to 351 ± 21 $Wm^{-1}K^{-1}$ was measured at RT using TDTR, about twice as large as previously reported BAs crystals.



▲ Figure 2: Carrier mobilities of BAs with varying carrier concentrations. The open and solid symbols represent the mobilities of holes and electrons, respectively.

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